REMARKS

Introduction

A three-month extension of time to respond to the May 20, 2005 Office Action is hereby respectfully requested. The Director is hereby authorized to charge $1,020.00 in payment of the three-month extension-of-time fee to Deposit Account No. 06-1075 (order no.: 099999.0099). A duplicate copy of this paper is enclosed herewith.

Claims 4 and 25-37 have been cancelled without prejudice. Claims 1, 5, 38, and 39 have been amended to more clearly and particularly define the invention. Claims 2, 3, and 6-24 are also in this case. No new matter has been added by the amendments to the claims.

Claims 1-3, 5-24, 38, and 39 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-3, 5, 6, 38, and 39 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Nolan et al. U.S. Patent 6,020,792 (hereinafter "Nolan") in view of Guedj U.S. Patent 6,118,315 (hereinafter "Guedj").

Reconsideration and allowance of this application in light of the following remarks is hereby respectfully requested.

Applicant's Reply
to the Rejection under 35 U.S.C. § 112

Claims 1-3, 5-24, 38, and 39 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In the aforementioned Office Action, the Examiner stated that the recitations "creates a very small difference in voltage" in each of claims 1 and 5 are indefinite because "it is not clear where in the circuit the 'very small difference in voltage' is created," (Office Action, page 2, lines 8 and 9). Applicant has amended each of independent claims 1 and 5 to more particularly point out and describe the claimed invention. No new subject matter has been added by these amendments.

Applicant has amended claim 1 to state that the first trigger signal "creates a small difference in voltage at the SET circuit," and that the second trigger signal "creates a small difference in voltage at the RESET circuit." Likewise, applicant has amended claim 5 to state that the first trigger signal "creates a small difference in voltage at the SET transistor," and that the second trigger signal "creates a small difference in voltage at the RESET transistor." The latch of each of applicant's claims 1 and 5 is shown, for example, in FIG. 2 by a SET circuit (e.g., circuit 225) and a RESET circuit (e.g., circuit 245). The SET circuit is shown having a first latch transistor (e.g., transistor 120) and a SET transistor (e.g., transistor 110), while the RESET circuit is shown having a second latch transistor (e.g., transistor 130) and a RESET transistor (e.g., transistor 140).

"To RESET latch 200, current is injected into RESET 195 to cause the base of transistor 140 to lift by about 18 millivolts (as opposed to the 700 millivolts signal required by conventional latches to change the latch output state). This small signal (referred to in this application as a current-driven signal because the change in voltage is so small) injected into the base of transistor 140 causes the base of transistor 140 to rise above a pre-determined value," (applicant's specification, page 8, lines 24-33). "Duplicating this circuit on the SET side produces a latch that is fully current driven, i.e., a signal that creates a very small difference in voltage (e.g., 18 millivolts) is sufficient to SET and RESET the latch. Thus, the operation time of such a latch is substantially reduced," (applicant's specification, page 9, line 26-31). Applicant respectfully submits, therefore, that the amendments to claims 1 and 5 overcome the indefinite rejection under 35 U.S.C. § 112 with respect to the term "creates a very small difference in voltage."

The Examiner further stated that claim 5 is indefinite because "it is not clear how at the first state a first current can be conducted by two transistors (first latch transistor and SET transistor) and at the second state how the same 'a first current' can be conducted by two other transistors (second latch transistor and RESET transistor)," (Office Action, page 2, lines 18-21). Applicant respectfully disagrees.

Applicant's claim 5 defines a latch including "a first latch transistor" (e.g., transistor 120 of FIG. 2), "a second latch transistor" (e.g., transistor 130 of FIG. 2), "a SET transistor" (e.g., transistor 110 of FIG. 2), and "a RESET transistor" (e.g., transistor 140 of FIG. 2). "When

the latch is SET, Q 170 is held high . . ., transistor 130 is ON and, therefore, transistor 140 is also ON because it is base-emitter coupled to transistor 130," (applicant's specification, page 8, lines 10-14.) "Thus, in this state, substantially the entire current generated by current sources 150 and 160 . . . is conducted by transistors 130 and 140," (applicant's specification, page 8, lines 14-18). Likewise, when the latch is RESET, ~~Q~~ 180 is held high, transistor 120 is ON and, therefore, transistor 110 is also ON because it is base-emitter coupled to transistor 120 (see, e.g., applicant's FIG. 7). In this state, substantially the entire current generated by current sources 150 and 160 is conducted by transistors 110 and 120. Therefore, it is clear how at the first state a total current (e.g., the total current generated by current sources 150 and 160) can be conducted by two transistors (e.g., first latch transistor 120 and SET transistor 110) and at the second state how the same total current can be conducted by two other transistors (e.g., second latch transistor 130 and RESET transistor 140).

The Examiner further stated that each of applicant's claims 38 and 39 is indefinite because the recitation the "trigger signal is more than an order of magnitude less than the full Vbe voltage" is confusing. Applicant has amended each of claims 38 and 39 to state the "trigger signal is less than the full Vbe voltage."

Therefore, the rejections of applicant's claims 1, 5, 38, and 39 under 35 U.S.C. § 112 are respectfully traversed. It follows that the rejections under 35 U.S.C. § 112 of claims 2, 3, and 7-24, which depend from claim 1, are also respectfully traversed. It similarly follows that the rejection under 35 U.S.C. § 112 of claim 6, which depends from claim 5, is also respectfully traversed.

Applicant's Reply
to the Rejections under 35 U.S.C. § 103

Claims 1-3, 5, 6, 38, and 39 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Nolan et al. U.S. Patent 6,020,792 (hereinafter "Nolan") in view of Guedj U.S. Patent 6,118,315 (hereinafter "Guedj").

Applicant's invention, as defined by amended claims 1 and 5, is for a latch. The latch of applicant's claims 1 and 5 is shown, for example, in FIG. 2 which includes a SET circuit (e.g., circuit 225) and a RESET circuit (e.g., circuit 245). The SET circuit is shown having a first latch transistor (e.g., transistor 120) and a SET transistor (e.g., transistor 110), while the RESET circuit is shown having a second latch transistor (e.g., transistor 130) and a RESET transistor (e.g., transistor 140). The output of the latch has a first state and a second state, and is controllable by the use of a "first trigger signal" which "creates a small difference in voltage" at the SET circuit and a "second trigger signal" which "creates a small difference in voltage" at the RESET circuit. Applicant has amended claim 1 such that "the SET circuit does not include a native transistor" and such that "the RESET circuit does not include a native transistor." Likewise, applicant has further amended claim 5 such that "the SET transistor is not

a native transistor" and such that "the RESET transistor is not a native transistor."

On page 3, lines 9-11 of the Office Action, the Examiner stated that "Nolan shows a latch circuit having an output (166), the output having a first state and a second state, the output being controllable by a first trigger signal (162) and second trigger signal (164)." However, "Figure 3 of Nolan does not show that the first and second trigger signals have very low threshold voltage. Guedj teaches that native transistors have very low threshold voltage close to zero volt (col. 5, lines 18-20). Therefore, it would have been obvious to an artisan having skills in the art to replace the input transistors of the set/reset circuit with the native transistors taught by Guedj for providing [the] fast latch circuit" of applicant's claims 1 and 5, (Office Action, page 3, lines 18-23).

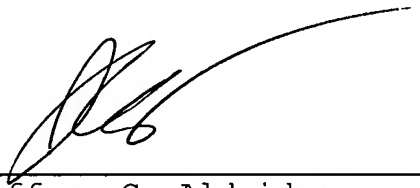
Nowhere does Nolan and or Guedj, alone or in combination, show or suggest a latch circuit whose output is controllable by first and second trigger signals each of which "creates a very small difference in voltage," as required by each of applicant's claims 1 and 5, wherein a SET circuit does "not include a native transistor" and wherein a RESET circuit does "not include a native transistor."

Thus, for at least these reasons, each of applicant's independent claims 1 and 5, and any claims dependent therefrom, including claims 2, 3, 6-24, 38, and 39, are allowable over Nolan in view of Guedj. Applicant respectfully requests, therefore, that the rejection of claims 1-3, 5, 6, 38, and 39 under 35 U.S.C. § 103(a) be withdrawn.

Conclusion

The foregoing demonstrates that claims 1-3, 5-24, 38, and 39 are allowable. This application is therefore in condition for allowance. Reconsideration and allowance are accordingly respectfully requested.

Respectfully submitted,



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